TRANSMITTAL SLIP

DATE 4 A[redacted]59

TO: R+D Lab

ROOM NO.	BUILDING
	B-25

REMARKS:

This is a [redacted] STAT proposal for semiconductor development which we are not buying. Technical discussion, however, may interest some of the transistor people at Lab [redacted] STAT Who would be interested? [redacted] STAT

FROM [redacted] STAT

ROOM NO.	BUILDING	EXTENSION

FORM NO. 241 REPLACES FORM 36-8

CONFIDENTIAL

50X1

50X1

TECHNICAL PROPOSAL NO. 176-S

Development of Silicon Transistor for a 30 Megacycle-10 Watt Oscillator

PREPARED FOR:

The Government & Industrial Div. 50X1

and

D. C. Labs

CONFIDENTIAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I

INTRODUCTION

This Technical Proposal is submitted in response to a request of D.C.Labs and the Government & Industrial Division [redacted] for the development of a silicon power transistor for a 30 megacycle-10 watt oscillator. 50X1

The contractor believes that a transistor of this type is feasible and can be fabricated by an extension of a variety of presently available techniques.

The proposed method of fabrication and the mathematical approaches to the design of this transistor are related in other portions of this proposal.

Objective specifications of the transistor appear as Appendix "A" of this proposal.

SECTION II

BACKGROUND

[redacted] Semiconductor Device Development Laboratories have developed and placed in production an extensive number of transistor types using a wide variety of transistor technologies. Semiconductor technology pertinent to the design of this transistor is the extensive knowledge of diffusion techniques gained by these laboratories in developing a family of microalloyed diffused base transistors in germanium and a family of shallow alloyed diffused base silicon transistors. Intensive studies by these laboratories of transistors made completely by diffusion techniques will play a most important role in the development of the proposed transistor. 50X1

At the disposal of this program are personnel greatly experienced in the techniques of precision masking by photoresist methods obtained as a result of [redacted] laboratories' work on color picture tubes for television. 50X1

The extensive experience of [redacted] in the field of high frequency transistors is widely known and will be utilized in this development program. 50X1

SECTION III

DESIGN CONSIDERATIONS

3.1 Introduction

Circuit design engineers have indicated that a 30 megacycle oscillator transistor with 10 watts output should have a reasonable beta at 2 amperes emitter current, and the collector junction should have a diode breakdown voltage greater than 60 volts.

3.2 Emitter Design

In order that the emitter have good injection efficiency at 2 amperes, empirical data indicates that an emitter area of 1600 $mils^2$ is required. In order that the entire emitter area have a fairly uniform degree of effectiveness as an emitter, the emitter shape should be a long, narrow strip. In order to keep the package small, this design calls for two emitter strips 8 mils x 100 mils separated by 8 mils, yielding a plateau area of 40 x 100 mils.

3.3 Base Design

The base will be graded from 0.01 Ωcm material at the surface to high resistivity n-type material, the diffused layer being approximately 0.3 mil thick.

In order to minimize the base resistance R_b', the emitter strips will be diffused through the diffused base with no more than .1 mil separating the emitter from the base.

This .1 mil separation will make the required emitter diode breakdown voltage possible. The narrow width of the separation

will make a low R_b' possible.

Because of this low R_b', the large collector capacitance is not important. (See Structure-Determined Gain-Band Product of Junction Triode Transistor, J. M. Early, Proceedings of IRE, December 1958, p.1924.)

3.4 f_{max}

On the basis of the above mentioned article,

$$f_{max} = \frac{1}{4\pi S}\left(\frac{3}{2R_{\square} C \tau}\right)^{1/2}$$

In our case,

S = 8 mils

$R_{\square}$ = about 120 ohms/square

C = about 4.4×10^{-15} farad/mil^2

$$\tau = \frac{1}{2\pi f_{c\alpha}} = 2.66 \times 10^{-9} \text{ sec}$$

$$f_{c\alpha} = \frac{D}{\pi W^2}\left(\frac{AV}{2KT}\right)^{3/2} = 60 \text{ mc/s}$$

Therefore, f_{max} = 320 mc/s.

f_{max} and $f_{c\alpha}$ will be made as high as possible, since the percent efficiency of the transistor as an oscillator approaches 100% at low frequency.

3.5 Power Gain at 30 Megacycles

On the basis of the above, it seems reasonable to expect a power gain of 28 at 30 megacycles.

3.6 Efficiency Considerations

If the oscillator works at 50% efficiency from a 30-volt supply, with an emitter current of 1.5 amperes and an emitter voltage of 0.7 volts, this transistor should have an AC power output of

about 15 watts. A top goal for this transistor would be 66% efficiency, i.e., 15 watts of D.C. in would yield 10 watts of A.C. out.

3.7 Depletion Layer Transit Time

The transit time in the depletion layer is about 2.5×10^{-10} sec. This will clearly not limit the frequency response.

3.8 Collector Breakdown Voltage and Punchthrough Voltage

With 0.5 mil thick high resistivity material in the collector barrier, there should be no problem in meeting a breakdown voltage and punchthrough voltage greater than 60 volts. The collector N+ grading will be made gradual, so that most of the depletion layer moves out into the collector region.

3.9 Thermal Considerations

The transistor should be able to dissipate about 15 watts for short duty cycles if the oscillator should become unloaded. The maximum junction temperature is 200°C. Therefore, if the ambient temperature gets to be no more than 45°C, the thermal resistance from the junction to the ambient must be approximately 10.3°C. Calculations show that the resistance of three mils of silicon between the junction and the stud is about 0.75°C. Calculations of the path through the walls indicate approximately 8°C/watt drop, and submount is about 0.9°C/watt. Thus, for these unloaded conditions, thermal drop can be maintained. A normal dissipation of up to 10 watts should be no problem. (See Figure 1 for the proposed package design.)

SECTION IV

PROPOSED METHOD OF FABRICATION

4.1 Introduction

As discussed in the Device Design Section, this transistor calls for an n-p i-n intrinsic structure utilizing diffusion techniques and a line structure.

4.2 Wafer Preparation

Wafers approximately 1" in diameter shall be cut from ingots pulled in a furnace utilizing the Czochralski technique. These ingots shall be pulled in the 1-1-1 plane and wafers shall be cut along the 1-1-1 plane within 1/2-degree. In diffusion work, the 1-1-1 plane results in less thermal etching than other crystal faces when exposed to the high temperatures necessary for diffusion.

The wafers shall be lapped to approximately 5 mils thickness on a Hoffman lapper. These wafers are then polished by lapping followed by a final chemical polish. These wafers are then ready for the initial phosphorus diffusion.

4.3 Initial Phosphorus Diffusion

The low value of collector resistance necessary for a power transistor will be obtained by doping a large portion of the collector to an N+ condition. After this diffusion, the wafer is returned to lapping.

4.4 Precision Lapping and Polishing

In order that the junctions formed by diffusion be flat and coplanar, the lapping and polishing techniques for conditioning the

surface prior to base and emitter diffusion must be very precise. Special equipment is used at Lansdale so that flat, coplanar surfaces can be lapped on silicon blanks on the order of one mil in thickness.

The phosphorus diffused blank is lapped on one side until approximately 3 mils thick. The blank is then precision lapped and polished. This operation leaves a narrow band of intrinsic material exposed.

4.5 Base Diffusion

After scrupulously cleaning the polished wafer, the base is formed by diffusing gallium into the intrinsic region. This diffusion forms the collector junction and grades the base region. The silicon oxide formed in this diffusion is used in subsequent operations.

4.6 Forming and Diffusing the Emitter

A Kodak photosensitive lacquer is applied to the wafer and then developed under an intense ultraviolet light source in all areas except the emitter strip region. This undeveloped photoresist is washed off to expose the oxide film. This oxide film is then removed with hydrofluoric acid. The developed photoresist is then dissolved off and the wafer again scrupulously cleaned.

The final diffusion is a carefully controlled diffusion of phosphorus to form the emitter junction and determine the base width. There is now a thinner oxide on the emitter than on the base region. This delineates the emitter strip. Now the emitter strip can be etched to the desired V_{EB} by carefully etching first with hydrofluoric

acid and then with a special hydrofluoric-nitric acid mixture.

4.7 Formation of the Plateau

In order to expose the collector junction and reduce the size of the collector area, the plateau is prepared. The wafer is treated with Kodak photosensitive lacquer; an indexed mask is placed over the wafer which has also been indexed, and the plateau area is developed symmetrically across the emitter and base strips. The surrounding undeveloped photoresist is removed, the surrounding oxide is removed, and the collector junction is exposed by etching with the special hydrofluoric-nitric acid solution.

4.8 Attachment to the Submount

The wafer is now scribed into individual plateau transistors. These are then soldered to a gold plated submount.

4.9 Electrode Attachment

Gold electrode leads are now affixed by thermal compression bonding at several points along the emitter and base strips in order to insure low lead resistance. These electrode leads are then attached to the stem leads.

4.10 Sealing

The mounted unit is chemically rinsed to assure a clean, stable surface. The unit is vacuum baked and then transported in a controlled atmosphere to a dry box containing a press. At this station, the unit is sealed in a controlled atmosphere by cold pressure welding.

4.11 Temperature Cycling and Final Testing

The finished transistor then undergoes a 100-hour temperature cycling, alternating between -65°C and +200°C. It is leak-checked

and then undergoes final testing for all important parameters.

SECTION V

ENGINEERING AND DELIVERY SCHEDULE

5.1 Phase A: Primary Research and Design - 3 Months

Intensive studies of present diffusion techniques will be undertaken in order to optimize the design for an oscillator of high collector efficiency. The design for maximum heat dissipation will be investigated and improvements over the present design will be incorporated. Any new equipment or modifications of existing equipment needed for the fabrication process will be acquired during this period.

5.2 Phase B: Initial Development - 3 Months

During this period, experimental units will be fabricated and evaluated to investigate any possible radical design changes that may be necessary. Any promising units will be supplied to the Philco Government & Industrial Division for evaluation.

5.3 Phase C: Final Development - 6 Months

During this period, improved experimental models of the transistor will be fabricated and tested, and a sufficient number of final development models will be supplied for evaluation and use by the Philco Government & Industrial Division.

Next 1 Page(s) In Document Denied

APPENDIX "A"

OBJECTIVE SPECIFICATIONS

BV_{CBO} (I_C = 50 μA)	60V
BV_{EBO} (I_C = 50 μA)	10V
Thermal Drop (infinite heat sink)	10°C/watt
Storage Temperature	200°C max.
I_{CBO} at V_{CBO} = 30V (at 25°C)	.5 μA
I_{EBO} at V_{EBO} = 1V (at 25°C)	.25 μA
f_{max} (V_{CE} = 10V, I_E = 2 ma)	120 mc
h_{fe} (I_C = 1 A, V_{CE} = 5V)	10 min.

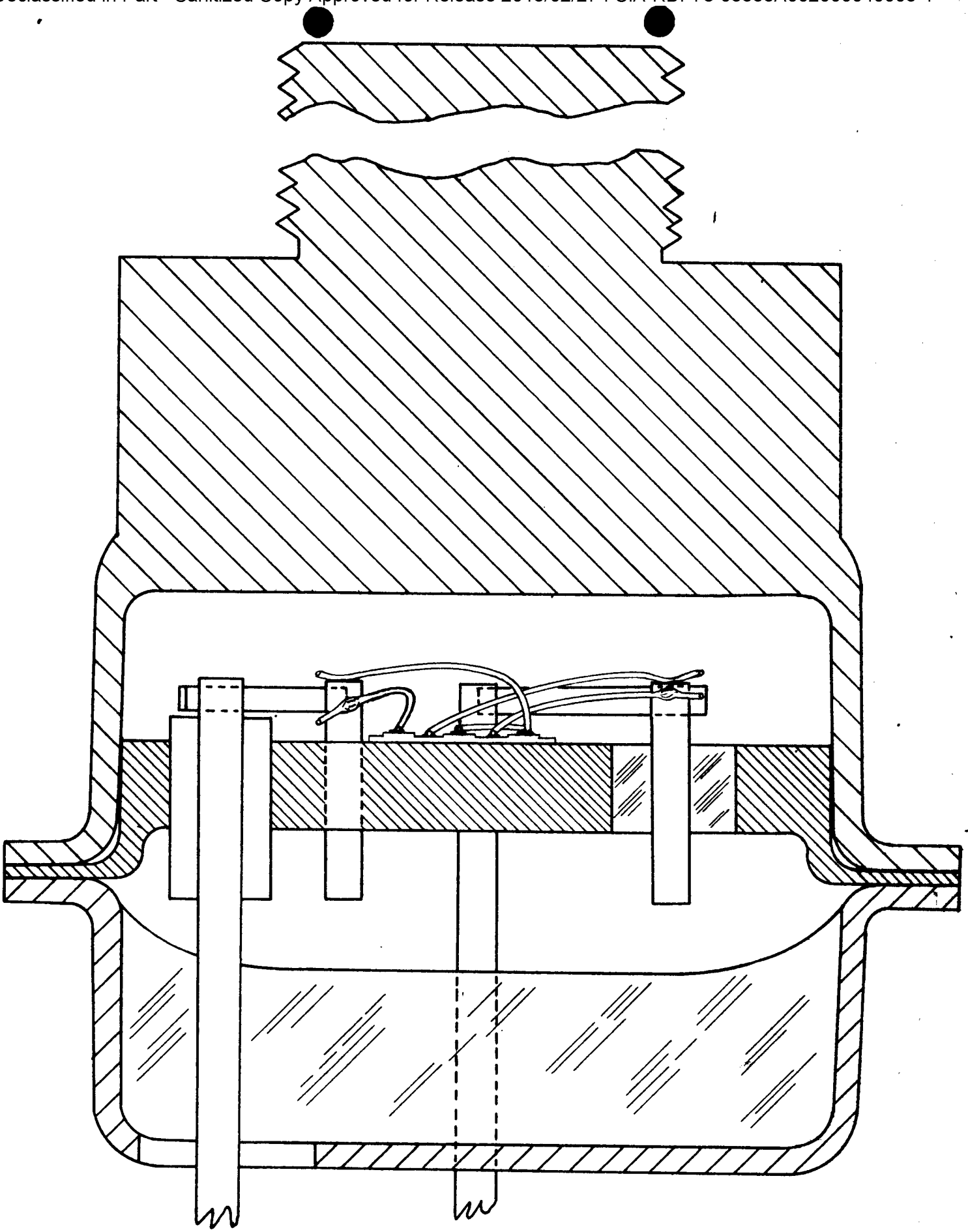

Figure 1. Mounted Transistor Cross-Section